REMARKS

1. Claims 1-50 were rejected under 35 U.S.C. 102(e) over U.S. patent no. 6,787,415 B1 to Chung et al.

1A. The last paragraph of Claim 1 recites a pedestal which "physically contacts two of the conductive lines". The examiner associates the applicants' pedestal with Chung's pedestal 340 (final office action of 10/10/2006, page 2). The examiner states in the advisory action of 12/22/2006:

> Figure 6, and col 3, lines 41-58, of Chung et al., illustrates, and teaches that the wordlines are in physical contact with the pedestal (the word lines **overlie** the pedestal)...

This is respectfully traversed. Chung's Fig. 6 shows two pedestals 340, and each pedestal 340 is overlain by only one wordline 160 (the wordline to the left of the respective pedestal). Thus, each pedestal 340 contacts only one wordline 160.

In the passage cited by the examiner (column 3, lines 41-58), Chung refers to multiple pedestals and multiple wordlines, but does not teach that a single pedestal may contact multiple wordlines.

Claims 2-50 are believed to be allowable for similar reasons.

1B. In addition, Claim 9 is believed to be allowable for the following reasons. Claim 9 depends from Claim 8 which depends from Claim 7 which depends from Claim 5 which depends from Claim 3 which depends from Claim 2 which depends from Claim 1. Claims 1, 2, 3, 5, 7, 8 and 9 recite in combination three etches of a first layer:

- a first etch of the first layer to form sidewall spacers (see Claim 1);

- an additional, second, anisotropic etch of the first layer (see Claims 3 and 9) which is performed to remove a portion P1 of the first layer (Claim 3). This is "a masked etch, with a portion of the first layer subjected to the second etch being defined by a photolithographic mask, wherein the same mask also defines a gate of a peripheral transistor" (Claim 5);

- a third, isotropic etch of the first layer over "second sidewalls" of first structures "but not over the first sidewalls" of the first structures (Claims 7 and 8).

Claim 9 is supported by the applicants' original disclosure as follows. The first layer reads on polysilicon 160 (Figs. 5A-5C). The first etch reads on the anisotropic etch described in paragraph 0041 (page 9) of the applicants' specification. This etch forms spacers shown in Figs. 6A, 6B. The second etch reads on the anisotropic etch of the polysilicon portions 160E, 160X2 (Fig. 7A) of layer 160 using a mask 410, as described on page 10, lines 4-5 and 18-20. The third etch reads on the isotropic etch of polysilicon portions 160S2 of layer 160 (Figs. 8A, 8F) using a mask 420, as described on page 11, paragraph 0054.

Chung discloses a spacer-forming etch of polysilicon 160 in column 5, lines 20-24, and another etch of polysilicon 160 in column 5, lines 27-31. The other etch removes the polysilicon spacers 160 from "the source line side of each row structure 280" and, possibly, removes some of polysilicon 160 "on the sidewalls of pedestals 340." Chung does not disclose the applicants' "second etch", which is in addition to the spacer forming etch and the etch of spacers 160 over "second sidewalls", and which uses a mask which also defines a gate of a peripheral transistor. The examiner states that the second etch is taught in Chung's "col. 4, lines 56-67, in col. 5, lines 1-25" (see page 3 of the final office action), but the etches described in column 4, lines 56-67 are etches of polysilicon layers 140, 120 and not of Chung's polysilicon 160 as in Claim 9. In fact, Chung's polysilicon 160 has not yet been formed at the stage described in column 4, lines 56-67. The etch described in col. 5, lines 1-25 is the spacer-forming etch described above.

Claim 29 is believed to be allowable for similar reasons.

2. New Claims 51-52 are dependent claims, supported by the applicants' specification, page 11, lines 18-19.

If a fee is required for this submission, please charge the fee or any underpayment thereof, or credit any overpayment, to deposit account 50-2257.

Any questions regarding this case can be addressed to the undersigned at the telephone number below.

Respectfully submitted,

Michael Shenker
Patent Attorney
Reg. No. 34,250

Law Offices of
MacPherson Kwok Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Tel: (408) 392-9250
Fax: (408) 392-9262